1   MICROPROCESSOR BASED SELF-DIAGNOSTIC PORT

2

3   BACKGROUND OF THE INVENTION

4

5   1. Field of the Invention

6   The invention relates to testing integrated circuits. More

7   particularly, the invention relates to an on-chip implementation

8   of a JTAG (Joint Test Action Group) master which can effect a

9   plurality of predefined tests of the chip without regard to other

10   devices on the same circuit board.

11

12   2. State of the Art

13   Over the years printed circuit boards (PCBs) have grown in

14   complexity. Advances in surface mount packaging and PCB

15   manufacturing have resulted in smaller PCBs with chips spaced

16   closer to each other than in the past. Thus, modern PCBs can not

17   always be tested with traditional tools, e.g. physical test probes

18   applied to the board externally.

19

20   In the 1980s, the Joint Test Action Group (JTAG) developed a

21   specification for boundary scan testing (BST) that was later

22   standardized as IEEE 1149.1. The BST can test pin connections

23   without the use of physical test probes. The BST standard defines

24   a serial protocol for accessing and controlling the signal-levels

25   on the pins of a digital circuit, and has some extensions for

1 testing the internal circuitry on the chip itself. All the

2 signals between the chip's core logic and its pins are intercepted

3 by a serial scan path known as the "Boundary Scan Register" (BSR).

4 In normal system operation this path can transparently connect the

5 core-logic signals to the pins and effectively become invisible.

6 In external-test mode, it can disconnect the core-logic from the

7 pins, drive the output pins by itself, and read and latch the

8 states of the input pins. In internal-test mode, it can

9 disconnect the core-logic from the pins, drive the core-logic

10 input signals by itself, and read and latch the states of the

11 core-logic output signals. The interface to the BST is via five

12 pins and an on-chip TAP (test access port) controller state

13 machine.

14

15   The JTAG interface uses the following five dedicated signals

16 which must be provided on each chip that supports the standard:

17   TRST, a Test-ReSeT input which initializes and disables the

18 test interface;

19   TCK, the Test CLocK input which controls the timing of the

20 test interface independently from any system clocks. TCK is pulsed

21 by the equipment controlling the test and not by the tested

22 device. It can be pulsed at any frequency (up to a maximum of

23 some MHz). It can be even pulsed at varying rates;

24   TMS, the Test Mode Select input which controls the

25 transitions of the test interface state machine;

1   TDI, the Test Data Input line, which supplies the data to the

2   JTAG registers (Boundary Scan Register, Instruction Register, or

3   other data registers); and

4   TDO, the Test Data Output line, which is used to serially

5   output the data from the JTAG registers to the equipment

6   controlling the test. It carries the sampled values from the

7   boundary scan chain (or other JTAG registers) and propagates them

8   to the next chip in the serial test circuit.

9

10   The normal organization of the test circuit on a board that

11   incorporates several chips with JTAG support is to connect TRST,

12   TCK, and TMS to every chip in parallel, and to connect TDO from

13   one chip to TDI of the next in a single loop. This presents a

14   single JTAG test interface for the board. It is possible to

15   provide individual access to each chip on the board but it would

16   require the use of five board pins for each chip.

17

18   Although the JTAG interface has proved to be very effective,

19   it is limited in some ways. First, in order to test a single chip

20   on a PCB is may be necessary to remove the chip from the board.

21   Although it is possible to test individual chips on a board

22   without removing them from the board, it is necessary to take the

23   board out of service to perform the tests. Further, in order to

24   implement JTAG tests, the board developer must be aware of various

25   parameters for each of the chips on the board.

1   On the chip level, JTAG has been used by manufacturers to

2 test a chip for compliance with the manufacturer's specifications.

3 It would be useful for board developers to be able to perform the

4 same tests that the chip manufacturer uses to determine whether

5 the chip is operating properly. It would also be desirable for

6 the chip manufacturer to provide the board developer with a turn-

7 key testing solution. These objects, however, are not easily

8 achievable. In order to provide a turn-key solution for a chip

9 which is being used on the developer's board, the chip

10 manufacturer would need to know the particulars about the board

11 and how the JTAG interface(s) are implemented on the board. This

12 is impractical because chip manufacturers want to make their chips

13 as versatile as possible so that they may be used on many

14 different board applications.

15

16   SUMMARY OF THE INVENTION

17

18   It is therefore an object of the invention to provide methods

19 and apparatus for enabling diagnostic testing of a chip on a

20 circuit board.

21

22   It is also an object of the invention to provide methods and

23 apparatus for enabling diagnostic testing of a chip on a circuit

24 board which do not require removing the chip from the board or

25 taking the board out of service.

1   It is another object of the invention to provide methods and

2 apparatus for enabling diagnostic testing of a chip on a circuit

3 board which enable the chip manufacturer to provide a single

4 testing solution for the chip which will work properly regardless

5 of the board on which the chip is used.

6

7   It is still another object of the invention to provide

8 methods and apparatus for selecting between standard JTAG testing

9 and testing according to the invention.

10

11   In accord with these objects which will be discussed in

12 detail below, the present invention provides an application

13 specific integrated circuit (ASIC) having a JTAG interface and a

14 microprocessor interface. According to the invention, the ASIC is

15 also provided with an on-chip JTAG master which is coupled to the

16 JTAG interface and the microprocessor interface. The

17 microprocessor interface is provided with a plurality of registers

18 which are mapped to the five JTAG signals and additional registers

19 which are used to conduct a plurality of tests. The methods of

20 the invention include controlling the on-chip JTAG master via an

21 off-chip microprocessor coupled to the microprocessor interface.

22

23   Using the invention, diagnostic tests of the chip can be

24 performed without removing the chip from the board and without

25 removing the board from service. Board developers and device

1 maintenance personnel can perform the same diagnostic tests as the

2 manufacturer to determine whether the chip is performing according

3 to specification. The invention therefore allows more accurate

4 tests of in-service boards which are part of a larger device, e.g.

5 a telecommunications switch. In addition, since the board does

6 not need to be taken out of service, the invention can be

7 advantageously used to create single chip systems. With the

8 invention, a chip manufacturer can supply developers with a set of

9 diagnostic programs which can be used to test the chip regardless

10 of how the board carrying the chip is designed. The present

11 implementation of the invention allows the same JTAG master and

12 microprocessor interface to be used on many different chips

13 without modification.

14

15   Additional objects and advantages of the invention will

16 become apparent to those skilled in the art upon reference to the

17 detailed description taken in conjunction with the provided

18 figures.

19

20   BRIEF DESCRIPTION OF THE DRAWINGS

21

22   Figure 1 is a high level block diagram of an ASIC according

23 to the invention; and

24

1   Figure 2 is a high level block diagram of a synchronization

2   circuit which is used to switch between the microprocessor control

3   of the JTAG TAP and traditional control of the JTAG TAP.

4

5   DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

6

7   Referring now to Figure 1, an ASIC 10 according to the

8   invention includes core logic 12 which provides the primary

9   functions of the ASIC and which is coupled to a plurality of pins

10   (not shown). In addition, the ASIC 10 is provided with a standard

11   JTAG TAP 14 which is coupled to the core logic 12 and selectively

12   coupled to the standard JTAG five pin interface TRST, TMS, TCK,

13   TDI, and TDO. According to the invention an on-chip JTAG Master

14   16 is selectively coupled to the JTAG TAP 14. The JTAG master 16

15   is coupled to an 8-bit microprocessor interface 20 via a plurality

16   of status and control registers 18.

17

18   More particularly the TDO output of the JTAG TAP is coupled

19   to a TDO input of the JTAG Master and via a switch 22 to the

20   standard TDO pin on the chip 10. The switch 22 is operated by

21   output from an OR gate 24 which receives input from both the JTAG

22   TAP (TDO output enable) and a select signal from the JTAG Master.

23   The JTAG master 16 outputs TRST, TMS, TCK, and TDI signals to a

24   switch 26 which is also coupled the TRST, TMS, TCK, and TDI pins.

25   The select signal from the JTAG Master 16 activates both switches

1 22 and 26 to override the JTAG pins on the chip and substitute the

2 JTAG Master for them. The JTAG Master also receives a select

3 reset signal from the TRST pin. As shown in the Figures, the

4 TRST, TMS, TCK, and TDI pins are each associated with an input

5 buffer 28, 30, 32, 34.

6

7   The status and control registers 18 include the following

8 registers identified in Table 1.

9

Register Name	MP Access	Function
TCK_Divider	R/W	A clock divider number (divisor) used to create a 10MHz TCK from the system clock
Counter	R/W	6-Bit shift count register.
TDI_FIFO_B0	R/W	Byte 0 of a (5x8 deep) FIFO containing TDI data to send to the TAP
TDI_FIFO_B1	R/W	Byte 1 of a (5x8 deep) FIFO containing TDI data to send to the TAP
TDI_FIFO_B2	R/W	Byte 2 of a (5x8 deep) FIFO containing TDI data to send to the TAP
TDI_FIFO_B3	R/W	Byte 3 of a (5x8 deep) FIFO containing TDI data to send to the TAP
TDI_FIFO_B4	R/W	Byte 4 of a (5x8 deep) FIFO containing TDI data to send to the TAP
TMS_FIFO_B0	R/W	Byte 0 of a (5x8 deep) FIFO containing TMS data to send to the TAP
TMS_FIFO_B1	R/W	Byte 1 of a (5x8 deep) FIFO containing TMS data to send to the TAP
TMS_FIFO_B2	R/W	Byte 2 of a (5x8 deep) FIFO containing TMS data to send to the TAP
TMS_FIFO_B3	R/W	Byte 3 of a (5x8 deep) FIFO containing TMS data to send to the TAP

TMS_FIFO_B4	R/W	Byte 4 of a (5x8 deep) FIFO containing TMS data to send to the TAP
TDO_FIFO_B0	R	Byte 0 of a (5x8 deep) FIFO containing TDO data received from the TAP
TDO_FIFO_B1	R	Byte 1 of a (5x8 deep) FIFO containing TDO data received from the TAP
TDO_FIFO_B2	R	Byte 2 of a (5x8 deep) FIFO containing TDO data received from the TAP
TDO_FIFO_B3	R	Byte 3 of a (5x8 deep) FIFO containing TDO data received from the TAP
TDO_FIFO_B4	R	Byte 4 of a (5x8 deep) FIFO containing TDO data received from the TAP
Start	R/W	Start bit is set to trigger a transfer between the microprocessor and the TAP via the JTAG Master. This bit clears the End bit.
End	R	When a transfer is completed, this bit is set.
JM_TRSTN	R/W	The value of TRST driven by the microprocessor interface. Initializes to logical '0'.
TDI_ Loop_Back	R/W	This bit loops back the TDI FIFO output, back into the TDO FIFO input. Used to test the interface.
TMS_Loop_Back	R/W	This bit loops back the TMS FIFO output, back into the TDO FIFO Input. Used to test the interface
TRSTN_Sample	R	This bit samples what the microprocessor interface is driving into the TAP
MP_CNTRL	R/W	This bit switches TAP control from pins to the on-chip JTAG master

Table 1

1

2

3   According to the presently preferred embodiments, the ASICs

4 according to the invention are designed for use in

5 telecommunications switching. These chips are generally provided

1 with a microprocessor interface which is connected to a host for

2 configuring the telecommunications switch, e.g. provisioning

3 circuits, establishing quality of services parameters, managing

4 queues, etc. The present invention makes use of this existing

5 microprocessor interface to control the new on-chip JTAG master

6 via the registers described above which coordinate the handshake

7 between the host processor and the JTAG master, and issue

8 instructions and operations to the target on-chip TAP state

9 machine.

10

11   Some of the features which are available via the

12 microprocessor interface include memory built-in self-test (BIST),

13 logic BIST, manufacturing ID codes, memory BIST diagnostic data,

14 special configuration registers, RAM repair information, etc.

15

16   Two FIFOs are used to control the TAP, the TDI FIFO and the

17 TMS FIFO. The TDI (test data input) FIFO is filled with the data

18 to be used in the test and the TMS (test mode select) FIFO is

19 filled with control information associated with each TDI bit that

20 will be applied to the TAP. The six-bit Counter is initialized

21 with the six-bit binary representation of the number of bits to be

22 shifted. As the TMS and TDI FIFOS are each 5x8, the maximum

23 number of bits to be shifted is forty. Once these three registers

24 are initialized, the Start bit is set and the JTAG master state

25 machine reads each bit from the TDI & TMS FIFOs, and places them

1   sequentially on the TDI and TMS inputs of the TAP. At the same

2   time, the JTAG master shifts TDO bits into the TDO FIFOs where

3   they can be read by the microprocessor. When the counter expires,

4   the End bit is set, and the last bit of the TMS register is held

5   on the TAP inputs.

6

7   According to the invention, the FIFOs are kept small to

8   conserve space on the chip. In the presently preferred embodiment

9   the FIFOs are no larger than 40 bits. However, by exploiting

10   features of the TAP standard, operations larger than 40 bits can

11   be achieved.

12

13   The TAP state machine is designed to allow four states to be

14   held in place without shifting in new data. These states, which

15   are held in place based on the TMS value, are as follows:

16   State 1: Test-Logic-Reset -- This clears all the internal

17   states of the TAP. Not used during test.

18   State 2: Run-Test-Idle -- This state is the 'No-Op'

19   equivalent for the TAP. No operation occurs, but active tests can

20   still be running inside the ASIC. This state will not interfere

21   with them, even though, the tests were initiated by the TAP.

22   State 3: Pause-IR -- This state is a pause in the shift of

23   the IR. From this state, the user has the option to go back to

24   shift the IR some more bits, or exit and update the IR.

1   State 4: Pause-DR -- This state is similar to the Pause-IR,

2   but used for the internal Data Register. So, by loading the TMS &

3   TDI fifos with a sequence of bits, the TAP can be cycled through

4   its state elements, and held into one of the above states,

5   depending on what needs to be done.

6

7   The following sequence, when loaded into the TMS & TDI FIFOs,

8   will take the TAP out of Test-Logic-Reset state and place it in

9   the Run-Test-Idle: state. It will also, hold the TMS to a value

10   of '1', which will keep the TAP in the Run-Test-Idle state.

11

12   TMS_Fifo: 00
13   TDI_Fifo: XX
14   Count: 2
15

16   The following sequence will load a sequence of 40-bits into

17   the DR register and read the 40 DR status bits into the TDO FIFO.

18   When the first operation is completed, the TAP will be held in the

19   Pause-DR state when TMS is '0', then next operation set will

20   complete the shift, and put the TAP back into the Run-Test-Idle

21   state (assuming it starts in the Run-Test-Idle state):

22

23   TMS_Fifo: 1000 0000 0000 0000 0000 0000 0000 0000 0000 0010
24   TDI_Fifo: XXX0 1234 5678 9012 3456 7890 1234 5678 9012 345X
25   Count: 40
26

27   The resulting state sequence is from Run-Test-idle to Select-DR-

28   Scan to Capture-DR to Shift-DR (36 times) to Exit1-DR to Pause-DR

1 (N times). This will pause the shifting of the DR for as long as

2 it takes the microprocessor to read the DR status bits from the

3 TDO FIFO and to initialize the next new transaction.

4

5   The following sequence will shift from Pause-DR to Exit2-DR

6 to Shift-DR (6 times) to Exit1-DR to Update-DR to Run-Test-Logic

7 (N times).

8

9   TMS_Fifo: 1000 0001 1000
10   TDI_Fifo: XX45 6789 XXXX
11   Count: 12
12

13 These operation sets are a subset of the full capability of the

14 TAP, but are sufficient to load/unload all the internal TAP states

15 including the IR and device ID registers.

16

17   The switching mechanism, shown generally in Figure 1 at 22,

18 24, 26, is designed to default to the normal JTAG interface. When

19 the microprocessor is to take control of the TAP, a signal

20 internal to the system is used to generate the switch. This

21 signal is identified as "Select" in the JTAG master 16.

22 Implementation of this signal may cause a problem if the system

23 has not been initialized, and a bad value might be issued that

24 makes the TAP inaccessible to the outside controls. Figure 2

25 shows the synchronization circuit that insures the proper

1   operation of both the normal JTAG TAP & the microprocessor interface.

2

3   As shown in Figure 2, the select signal from the JTAG master

4   16, which is controlled by the contents of MP CNTRL REGISTER 18',

5   is NORed with a board level test pin. In Figure 2 this pin is

6   labeled "HIGH Z", but any other board level test pin could be

7   used. This pin is normally asserted (driven to 0) when the chip

8   is operational. The circuit behaves in the following manner:

9   For tests run on the tester, the tests will strictly rely on

10   the TAP being driven from the primary I/O pins. By asserting the

11   HIGH Z pin to 1, the output of the NOR gate will always be 0,

12   causing the standard JTAG interface to control the TAP. This

13   requires that the HIGH Z pin be considered an IEEE 1149 compliance

14   pin during any JTAG activity, while the ASIC is in stand alone

15   mode.

16

17   For tests run in a system, tests will require that the HIGH Z

18   pin be driven to 0, and the MP CNTRL REGISTER will select the

19   source controlling the TAP. The MP CNTRL REGISTER is initialized

20   to 1 with the microprocessor interface at the time the

21   microprocessor interface is initialized. As such, the in-system

22   TAP will default on power up to control by the external pins, and

23   can be selected by the microprocessor to be controlled by on board

24   signals from the JTAG master.

25

1   A prototype of the invention was synthesized for 0.18μm and

2 0.13μm TSMC Artisan Libraries. The resulting area of this block

3 is approximately 5000 gates which represents a very minimal area

4 overhead in the state of the art.

5

6   Referring once again to Table 1, the microprocessor interface

7 can also be tested for correctness of operation. The interface

8 can be placed into loop-back where either the TMS FIFO or the TDI

9 FIFO is fed into the TDO FIFO. This loop back scheme allows the

10 microprocessor interface to fully test bus accesses and the FIFOs

11 used to drive the TAP. TRST can be sampled through the

12 TRST_sample register, and its value confirmed.

13

14   There have been described and illustrated herein an

15 integrated circuit with an on-chip JTAG master coupled to a

16 microprocessor interface. While particular embodiments of the

17 invention have been described, it is not intended that the

18 invention be limited thereto, as it is intended that the invention

19 be as broad in scope as the art will allow and that the

20 specification be read likewise. It will therefore be appreciated

21 by those skilled in the art that yet other modifications could be

22 made to the provided invention without deviating from its spirit

23 and scope as so claimed.

24